Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUTPUT 1**
2. **GND 1**
3. **+INPUT 1**
4. **–INPUT 1**
5. **V-**
6. **OUTPUT 2**
7. **GND 2**
8. **+INPUT 2**
9. **–INPUT 2**
10. **V+**

**.079”**

**1 10 9 8 7**

**119**

**MASK**

**REF**

**.059”**

**6**

**2 3 4 5**

**NOTE: CHIP BACK MUST BE CONNECTED TO V-**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: 119**

**APPROVED BY: DK DIE SIZE .059” X .079” DATE: 7/11/22**

**MFG: LINEAR TECH THICKNESS .015” P/N: LM119**

**DG 10.1.2**

#### Rev B, 7/1